CLAIMS

We claim:

1. A structure for testing external connections to semiconductor devices, the structure comprising:

an external electrical path between selected external connections on the semiconductor devices.

2. The structure according to claim 1, wherein the external electrical path comprises a thin film interface probe.

3. The structure according to claim 1, wherein the external electrical path [permits] interfaces a driver from an input/output to [interface to] a receiver of a corresponding paired input/output.

4. The structure according to claim 1, wherein the external connections on the semiconductor devices are C4 connections.

5. The structure according to claim 1, wherein the

structure carries out boundary scan and input/output wrap test techniques.

6. The structure according to claim 1, wherein all adjacent input/output pairs are paired.

7. The structure according to claim 1, wherein the structure provides a high frequency closed loop self test of drivers and receivers.

8. The structure according to claim 1, wherein the structure is extendible to full wafer contacting for burn-in and test.

9. The structure according to claim 1, wherein the external electrical path comprises:

a thin film of electrically insulating material;

a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;

electrically conducting material arranged in the plurality of passages; and

electrical connections between the electrically conducting material in selected pairs of the plurality of passages.

10. The structure according to claim 9, further comprising:

a space transformer connected to the electrically conducting material arranged in the plurality of passages.

11. The structure according to claim 1, wherein the external electrical path is provided between pairs of external connections on the semiconductor devices.

12. The structure according to claim 1, wherein the external electrical path is provided between a plurality of external connections on the semiconductor devices.

13. The structure according to claim 1, wherein the external electrical path is provided between non-adjacent external connections on the semiconductor devices.

14. A method for testing external connections to a semiconductor device, the method comprising:

providing an external electrical path between selected external connections on the semiconductor devices; and

carrying out the testing by sending at least one signal through the external electrical path.

15. The method according to claim 14, wherein the test comprises at least one of a boundary scan and input/output wrap test.

16. The method according to claim 14, further comprising:

pairing all adjacent input/output pairs.

17. The method according to claim 14, wherein the test comprises a high frequency closed loop self test of drivers and receivers.

18. The method according to claim 14, wherein the test comprises burn-in.

19. The method according to claim 14, further comprising:

interfacing a driver from an input/output to a receiver

of a corresponding paired input/output.

20. The method according to claim 14, wherein providing the external electrical path comprises:

providing a thin film of electrically insulating material;

providing a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;

providing electrically conducting material arranged in the plurality of passages; and

providing electrical connections between the electrically conducting material in selected pairs of the plurality of passages.

21. The method according to claim 20, further comprising:

providing a space transformer connected to the electrically conducting material arranged in the plurality of passages.

22. The method according to claim 14, wherein the

external electrical path is provided between pairs of external connections on the semiconductor devices.

23. The method according to claim 14, wherein the external electrical path is provided between a plurality of external connections on the semiconductor devices.

24. The method according to claim 14, wherein the external electrical path is provided between non-adjacent external connections on the semiconductor devices.

25. A method for forming a structure for testing external connections to semiconductor devices, the method comprising:

providing a thin film of electrically insulating material;

providing a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;

providing electrically conducting material in the plurality of passages; and

providing electrical connections between the

electrically conducting material in selected passages.

26. The method according to claim 25, wherein providing the electrical connections between the electrically conducting material in the selected passages comprises providing electrically conducting material on the thin film of electrically insulating material between the selected passages.

27. The method according to claim 25, wherein the selected passages are adjacent pairs.

28. The method according to claim 25, wherein the electrical connections are provided between a plurality of passages.

29. The method according to claim 25, wherein the electrical connections are provided between non-adjacent passages.